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MODELLING AND DESIGN OF A NOVEL MULTILEVEL INVERTER FOR A GRID CONNECTED PHOTOVOLTAIC SYSTEM

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ABSTRACT

A five level inverter and a nine level inverter are designed for a grid connected photovoltaic system to achieve a better performance by reducing the switching losses, harmonic distortions due to the switching operations.The five level inverter requires two capacitors supplying dc voltage to a dual buck converter which gives a three level dc voltage, this three level dc is fed to single phase full bridge inverter of which all the switches are operated in low frequency synchronous to utility voltage. A nine level inverter can be designed by using two dual buck converters supplied by four balanced dc capacitors of same voltage, single phase full bridge inverter. The input to the single phase full bridge inverter is a five level dc supplied from dual buck converters, which gives a nine level ac voltage as output. The output current of both the inverters is controlled to be a sinusoidal current in phase to the utility voltage.

KEYWORDS: Inverter, Voltage Balance, Dual Buck Converter

INTRODUCTION

The multilevel inverters are more advantageous compared to the conventional two level inverters where higher ratings of the semiconductor switches are required to produce higher voltages [1]-[2]. The multilevel inverter structure offers lower voltage stresses on the switching devices. The three main topologies of multilevel inverters are Diode clamped multilevel inverter, flying capacitors multilevel inverter, cascaded H-bridge multilevel inverter [3], [6].

In diode clamped multilevel inverter, for the output phase voltage to be n-level, it requires (n-1) dc capacitors, 2(n-1) switches, (n-1)(n-2) diodes. Though it a benefithigher efficiency as all the switches are operated at fundamental frequency at the rate of simple control technique.It faces disadvantages like the need of more number of switches, the difficulty in balancing the capacitor voltages. In flying capacitor multilevel inverter, for a n-level converter with an output phase voltage of n-level and line voltage of (2n-1), it requires $\Sigma^{n}_{i=1}$ (n-i) dc capacitors. The need of large number of capacitors makes it difficult in balancing these capacitor voltages. Though cascaded H-bridge inverters need less no of components, for n-level inverter it requires (n-1) number of full bridges but, main drawback of the is that they require separate dc sources which limit its application [3],[5].

So this paper presents newly developed topologies of five level inverter and nine level inverters, in which five level inverter requires 6 switches, 2 diodes, 2 dc capacitors in order to generate a five level output. This can be extended as a nine level inverter which requires 8 switches, 4 capacitors, 3 diodes. Thus, these new topologies solves the complexities as seen in the conventional multilevel inverters.

Novel Multilevl Inverter Topology

Figure 1 and **Figure 2** show the schematic of five level inverter and nine level inverter. The five level inverter consists of a dc source which can be obtained from solar cell arrays, dual buck converter of two switches S_2 andS_3, two capacitors of equally balanced voltages. This dual buck converter gives a three level dc voltage which is fed to the single phase bridge inverter to get the five level voltage. The nine level inverter is designed by using two more capacitors and two more switches $S_{8,}S_9$as shown in the **Figure 2**.

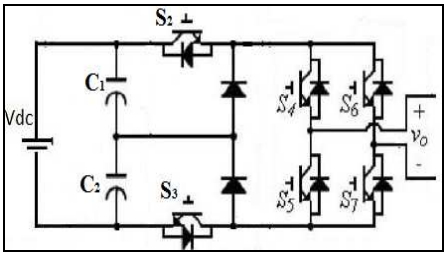

Figure 1: Schematic of Five Level Inverter

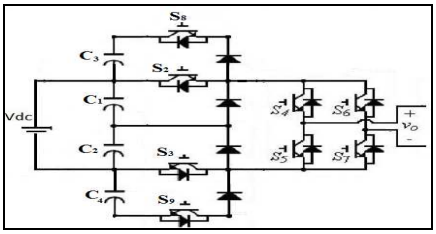

Figure 2: Schematic of Nine Level Inverter

- **Five Level Inverter**

There are eight modes of operation in the five level inverter, in which four modes contribute to the positive half cycle of the output voltage and the other four modes for the negative half cycle. Switches from S_2 to S_7 operate in these modes. The operation of switches S_2 and S_3 defines the voltage magnitude of three level dc which is the input to the single phase full bridge inverter. When both the switches are in ON, the total dc voltage stored in the two capacitors appears as the input to the full bridge inverter. If any one of the switches is under ON only the respective dc capacitor voltage is half of the dc voltage. If both the switches S_2 and S_3 are OFF then the output voltage will be Zero. Both the switches S_2 and S_3 are to be operated either in high frequency or in completely ON state in such a way that always the output voltage must be higher than the absolute value of the utility voltage. The switching operation of switches $S_{4,}S_{5,}S_{6,}$S7 gives a five level ac. All these switches $S_{4,}$ S5, S6, S7 are to be operated with switching frequency same as the fundamental frequency of the utility voltage.

The different modes of operations and their respectiveoutput voltage levels can be explained below. In mode 1, switches S_2,S_3, S_4,S_7 are under ON state and switches S_5,S_6 are OFF. This gives an output voltage of magnitude V_{dc}, where $V_{dc}$is the total dc stored in the two equally balanced capacitors. full bridge inverter gives the five level output of which the five levels are $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}$ /2,$-V_{dc}$. In mode 2, switches S_2,S_4,S_7 are under ON state and switches S_3, S_5,S_6 are OFF. This gives an output voltage of magnitude $V_{dc}/2$. In mode 3, switches S_3, S_4,S_7 are under ON state and switches S_2,S_5,S_6 are OFF. This gives an output voltage of magnitude V_{dc} /2. In mode 4, switches S_4,S_7 are under ON state and switches S_2, S_3,S_5,S_6 are OFF. This gives an output voltage of magnitude is zero. Thus, the modes of operation from (1-4) modes gives

the positive half cycle of the output voltage. Similarly the negative half cycle of the output voltage can be obtained from the remaining modes of operation.

- **Nine Level Inverter**

The nine level inverter can be considered as the extension of the above mentioned five level inverter. It requires another 2 switching devices, two capacitors, in addition compared to that of the five level inverter. In this all the capacitors are to be balanced with an equal dc voltage $V_{dc}/4$. The switches S_2,S_3, S_8,$S_9$are to be operated in high frequency which defines the five levelled dc output supplied to the single phase full bridge inverter. The switches S_4,S_5, S_6,S_7 are operated in low switching frequency same as the fundamental frequency of the utility voltage. When all the switches S_2,S_3, S_8,S_9 are at ON state the output is V_{dc}, if any three of these switches are at On state the output is $3V_{dc}$ /4, if any two of these switches are in ON state the output is $V_{dc}/2$, if only one of these switches ais in ON state the output is $V_{dc}/4$,if all the switches are at OFF state then the output is zero. Thus, the five levelled dc is obtained and is supplied as input to the full bridge inverter which gives the nine level output. If the switches S_4,S_7 are at ON then the positive half cycle appears at output and if S_5, S_6 are at ON then negative half cycle appears at the output.The obtained nine levels of output are $+V_{dc,}$ $+3V_{dc}$ /4, $+V_{dc}/2$, $+V_{dc}$ /4,0, $-V_{dc}$ /4, $-V_{dc}/2$, $-3V_{dc}$ /4, $-V_{dc.}$

Voltage Balance of the Capacitors:

In order to obtain a symmetrical ac voltage wave as output the dc capacitors in the dc bus side must be properly balanced with equal voltages. Also the capacitor voltage must be greater than the absolute value of the utility voltage at any given instant. For these conditions to be satisfied, in case of five level inverter switches S_2,S_3 are to be controlled and in case of nine level inverter switches S_2,S_3, S_8,S_9 are to be controlled. In five level inverter,when the absolute value of the utility voltage is less than $V_{dc}/2$ that is the capacitor voltage, then any one of the two switches S_2,S_3 is to be switched ON or in high frequency and the other switch is OFF. The choice of the switch whether it is to be switched ON or OFF depends upon the voltage levels of the two capacitors withrespective to the switches. If V_{c2} (the dc capacitor C_2 voltage) is greater than V_{c3} (the dc capacitor C_3 voltage) then the switch corresponding to capacitor C_2 i.e. S_2 must be switched in high frequency. So that, the high voltage capacitor c_2 gets discharged and its voltage gets balanced to that of the other capacitor voltage. In the other hand if the V_{c3} is greater than V_{c2} then the switch corresponding to capacitor C_3 i.e. S_3 must be switched in high frequency.

In the other case where the absolute value of the utility voltage is greater than $V_{dc}/2$, then one of these switches must be switched at high frequency and the other is to be at ON state, where the switch corresponding to higher voltage capacitor should be ON and the other is to be at high frequency. Thus the capacitor balance is achieved. In nine level inverter the same control strategy is to be applied as seen above. when the absolute value of the utility voltage is less than $V_{dc}/2$ then any of the required switches among S_2,S_3, S_8,S_9 are to switched in high frequency and the other switches are to be at OFF state depending upon the magnitude of five level dc output. Further, the switch selection is done with respect to the voltages of the capacitors. Hence the voltages of the capacitors get balanced. In the other case where the absolute value of the utility voltage is greater than $V_{dc}/2$, then one of these switches must be switched at high frequency and the other is to be at ON state, where the switch corresponding to lower voltage capacitor should be switched at high frequency and the other is to be ON.

Control Strategy

The main criteria in the inverter system is the dc bus voltage must be higher than the absolute value of the utility voltage; The capacitor voltages must be equal, the inverter must generate a sinusoidal current in phase with the utility voltage. For these to be satisfied the following sequence of control operations are to be made for novel multilevel topologies.

- **Five Level Inverter**

The control block of five level inverter for generation of switching signals is as shown in **Figure 3** and described below.The voltages of V_{c2} andV_{c3} are added to get the dc bus voltage $V_{dc.}$ A constant dc voltage is set which is greater than the peak of the utility voltage. The difference of these two dc voltages is measured and sent to the PI controller in order to monitor the condition whether the dc bus voltage is be greater than the absolute value of the utility voltage at any given instant. In order to identify islanding operation, the rms value of the utility current is measured and is sent to the hysteresis comparator which compares the utility current with a threshold value. For a normal operation always the utility current must be greater than higher threshold value, here the output signal of hysteresis comparator is low. In the case of islanding operation where the utility current is lower than lower threshold value and the output signal of comparator is high.

The outputs of both the hysteresis comparator and the PI controller are sent to multiplier which in turn gives the magnitude of reference signal. The utility voltage is measured and sent to the phase locked loop so that it produces a unity magnitude sine wave which is in phase with the utility voltage. The outputs of both these multiplier and phase locked loop are sent to another multiplier which generates a reference wave of the output current of the five level inverter. The output current of the five level inverter is compared with the generated reference current wave and the result is sent to the controller which has to control the PWM circuit to produce a PWM signal.The voltages of these two capacitors are sent to comparator which gives an output signal (S_a) with respect to the voltage levels of these capacitors, in addition to this the absolute of utility voltage is compared to $V_{dc}/2$ which generates another signal (S_b). the output of PWM circuit and the two signals $S_{a,}S_b$ are sent to the mode selection system. To a comparator the measured utility voltage is given so that it gives square wave reference signals that are complementary which control the switches of full bridge inverter.

- **Nine Level Inverter**

Due to the additional components S_8,S_9 and C_3, $C_{4;}$ the control scheme slightly varies in obtaining the criteria of balanced capacitor voltages and maintaining the absolute of utility voltage lower than half of dc bus voltage. Here there are four capacitor voltages which are to be maintained with equal voltages. Hence, all these capacitor voltages are to be compared. In order to get a proper islanding detection and achieving an output sinusoidal current in phase with the utility voltage, the control technique is same as in case of five level inverter as mentioned above. The control block of nine level inverter is shown in Figure 4.

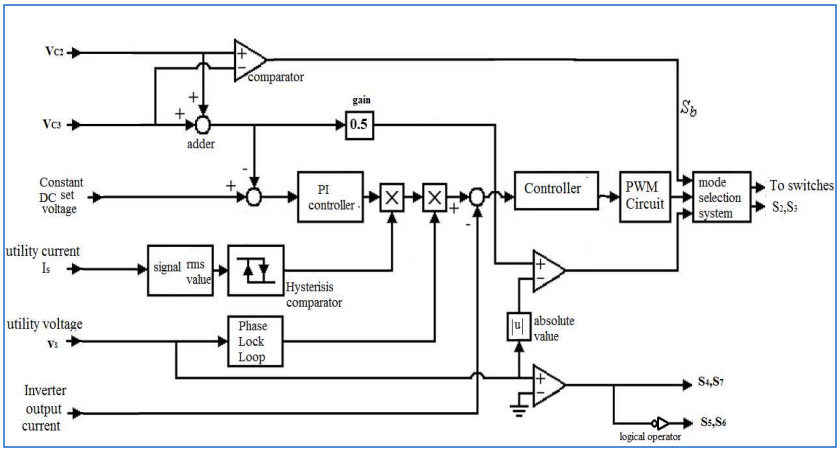

Figure 3: Control Block of Five Level Inverter

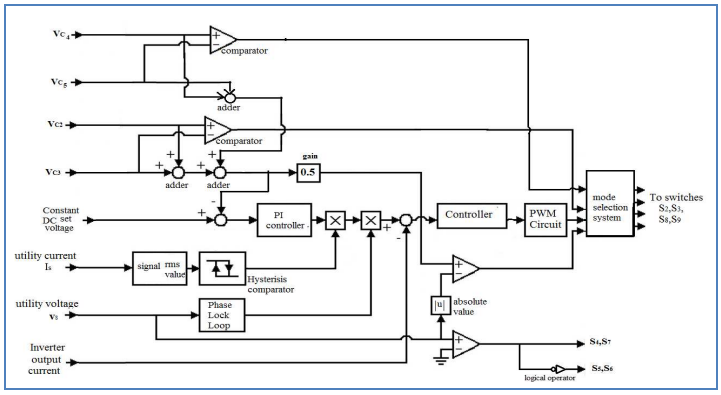

Figure 4: Control Block of Nine Level Inverter

SIMULATION RESULTS

The Figure 5.1 to 5.2 show the phase voltage, three level dc voltage of dual buck converter, output current of the five level inverter and Figure 6.1 to 6.2shows the output phase voltage, five level dc voltage supplied to full bridge, output current of the nine level inverter for an utility voltage of 110V ac and the input dc of 165 volts. The THD of the five level output voltage is found as 4.77%, the THD of the nine level output voltage is 2.52%.

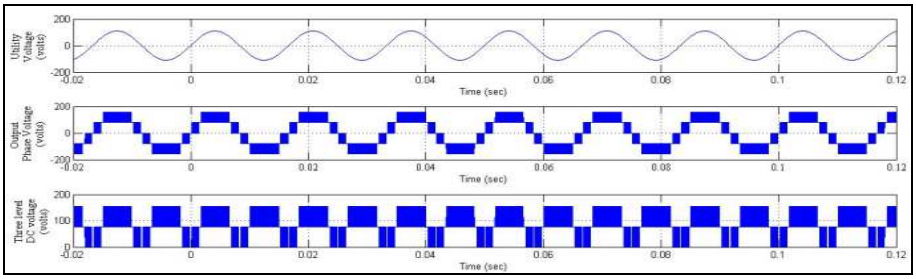

Figure 5.1: (a) Utility Voltage,(b) Output Phase Voltage,
(c)Three Level DC Output, of Five Level Inverter Topology

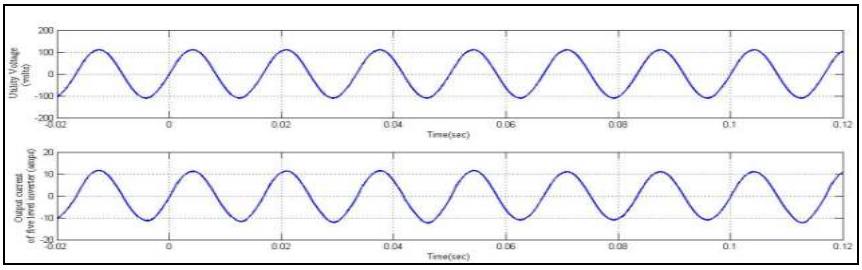

Figure 5.2: (a) Utility Voltage,(b) Output Current of Five Level Inverter

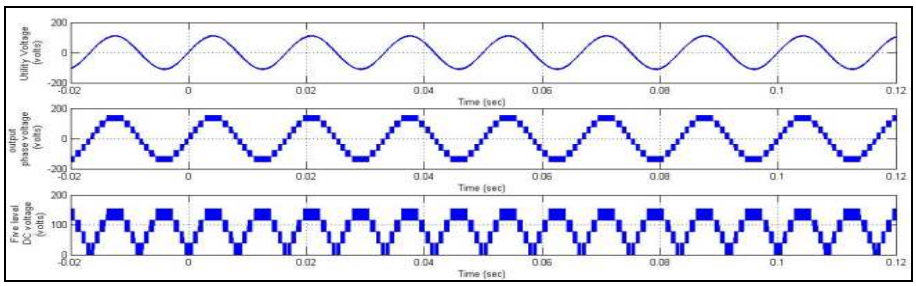

Figure6.1: (a) Utility Voltage,(b) Output Phase Voltage,(c) Five Level DC, of Nine Level Inverter

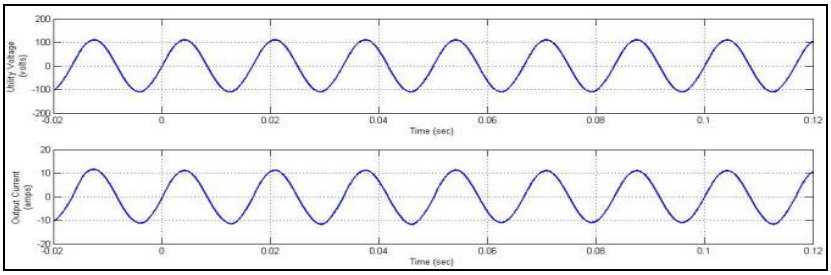

Figure 6.2: (a) Utility Voltage,(b) Output Current of Nine Level Inverter

CONCLUSIONS

Novel topology based five level inverter and a nine level inverter are developed for a grid connected photovoltaic system and a better performance is achieved with a lower THD value, proper balancing of capacitor voltages is done and a sinusoidal current in phase to the utility voltage is achieved.

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